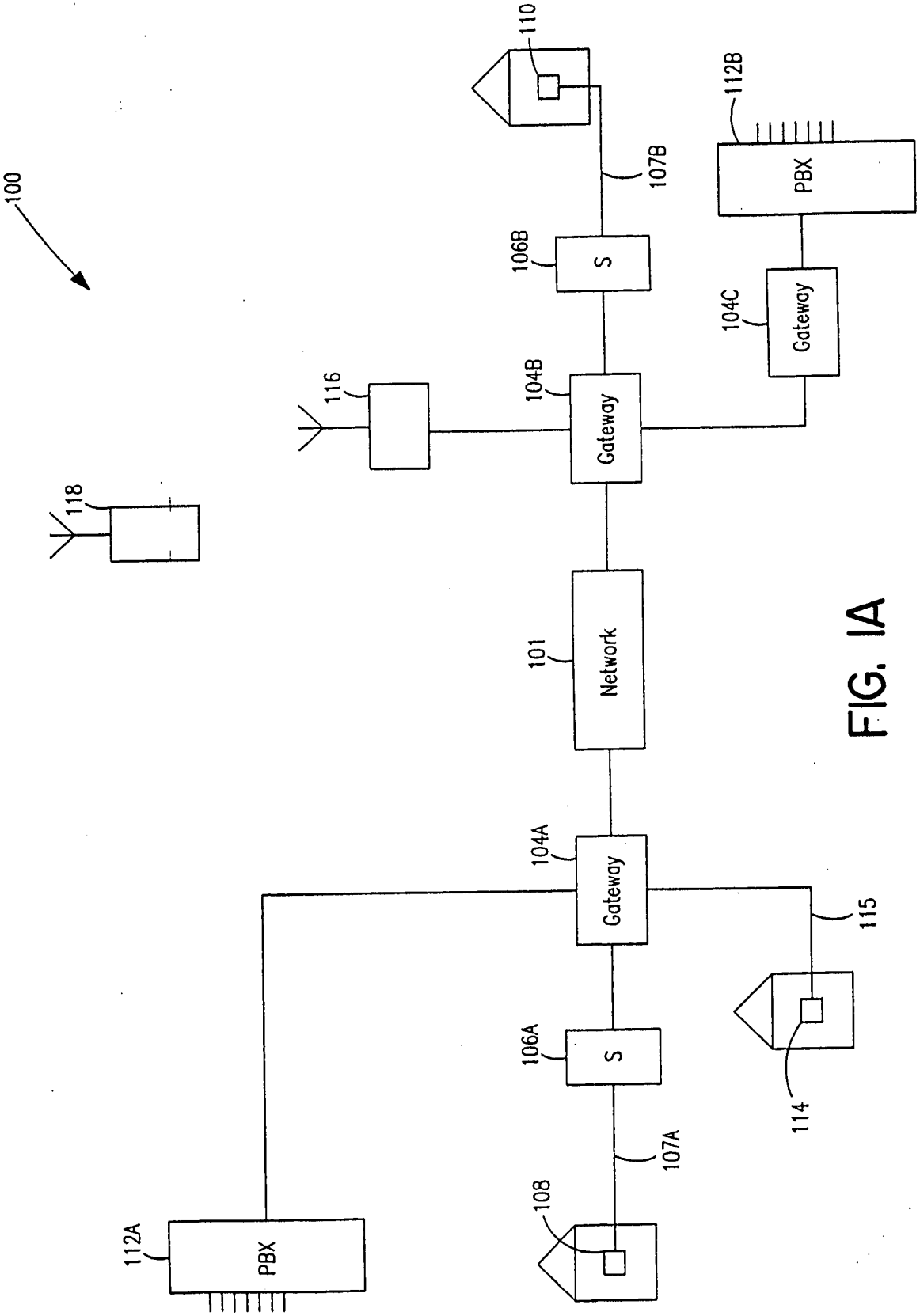

FIG. 1A

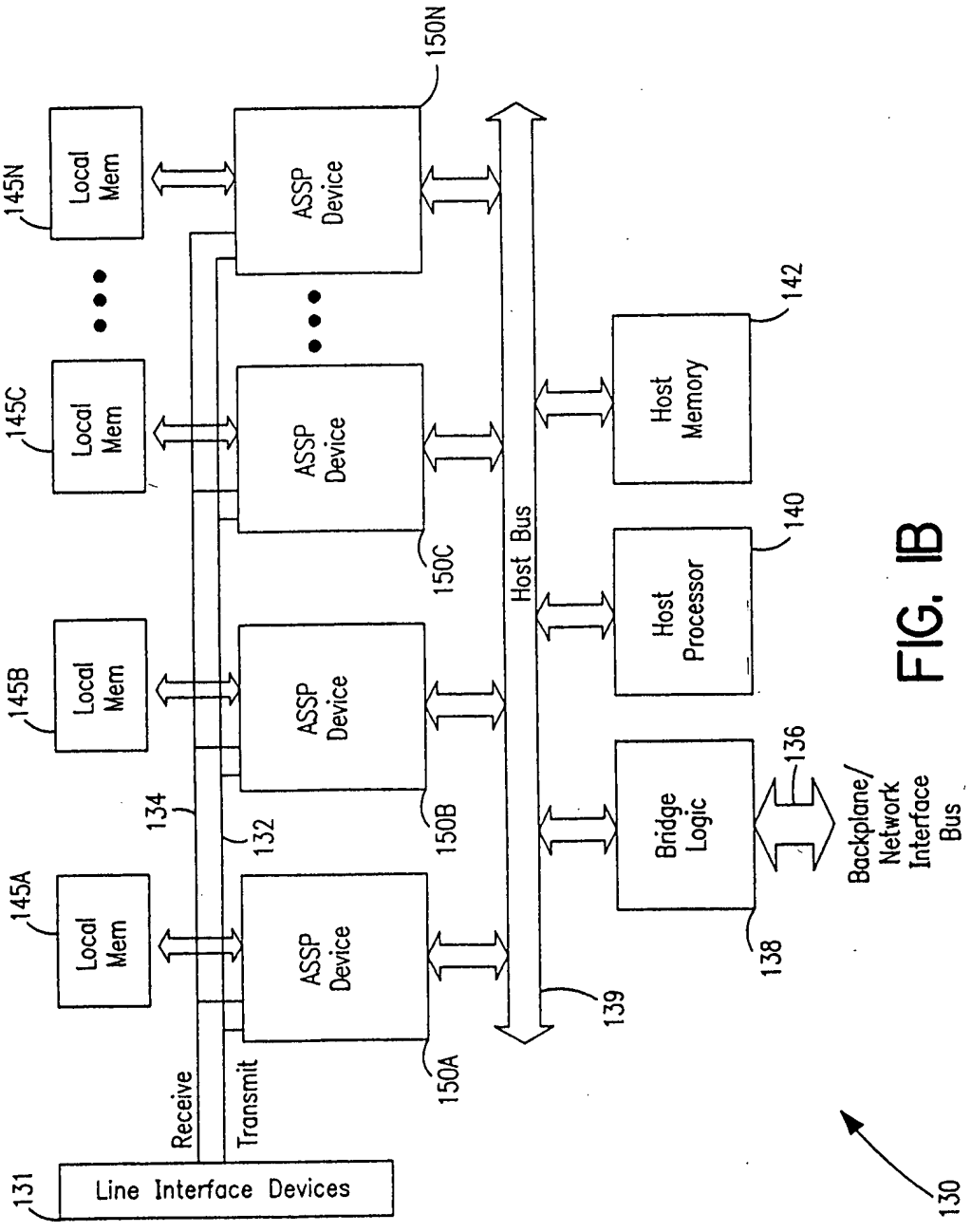
150N
145N
Local Mem
ASSP Device
142
Host Memory
145C
Local Mem
ASSP Device
150C
Host Bus
140
Host Processor
145B
Local Mem
ASSP Device
150B
134
132
136
Bridge Logic
Backplane/ Network Interface Bus
145A
Local Mem
ASSP Device
150A
139
138
Receive
Transmit
131
Line Interface Devices
130

FIG. 1B

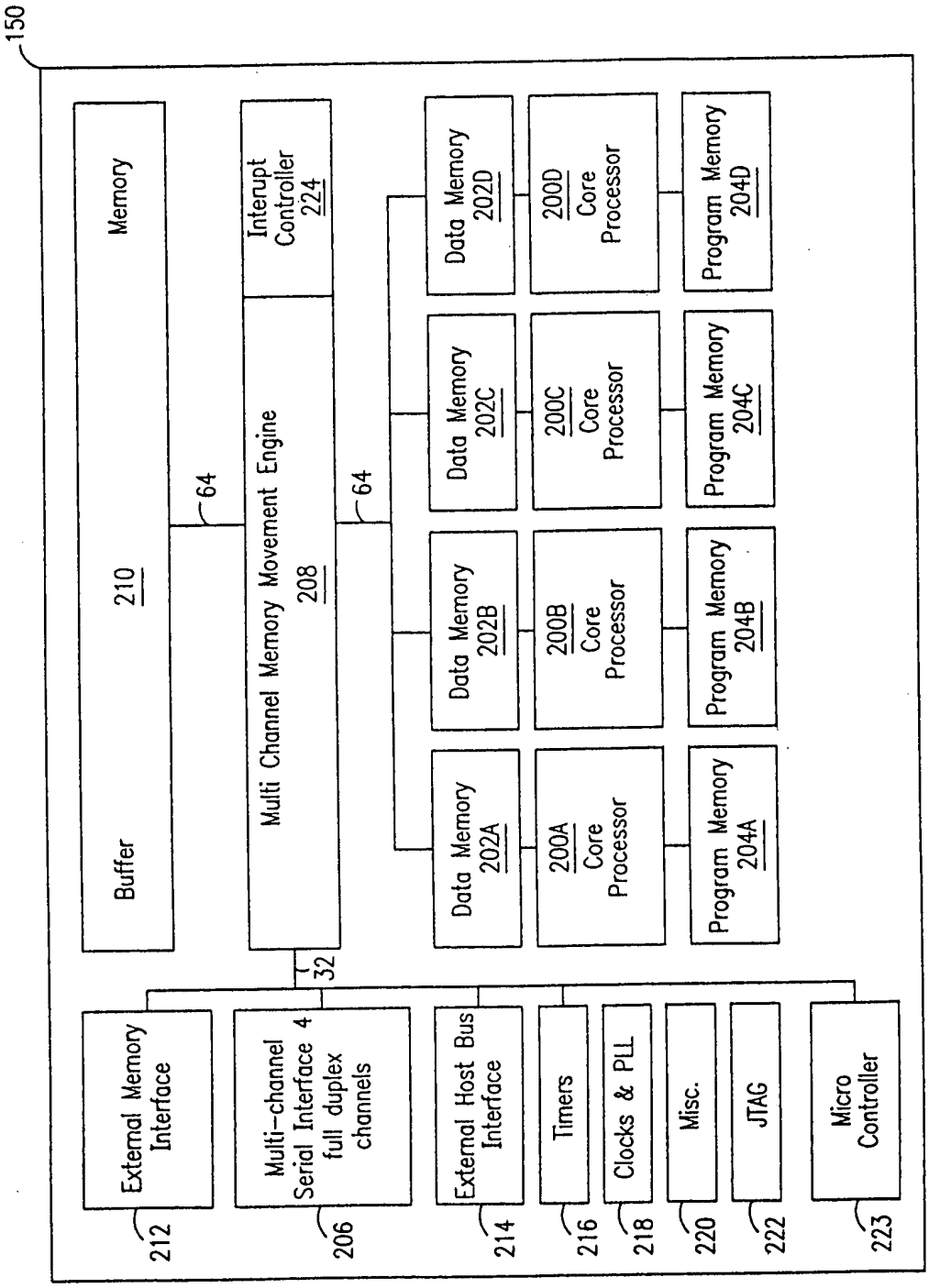
150
Memory
Buffer
210
64
Interupt Controller 224
Multi Channel Memory Movement Engine 208
64
Data Memory 202A
Data Memory 202B
Data Memory 202C
Data Memory 202D
200A Core Processor
200B Core Processor
200C Core Processor
200D Core Processor
Program Memory 204A
Program Memory 204B
Program Memory 204C
Program Memory 204D
32
External Memory Interface
212
Multi-channel Serial Interface 4 full duplex channels
206
External Host Bus Interface
214
Timers
216
Clocks & PLL
218
Misc.
220
JTAG
222
Micro Controller
223

FIG. 2

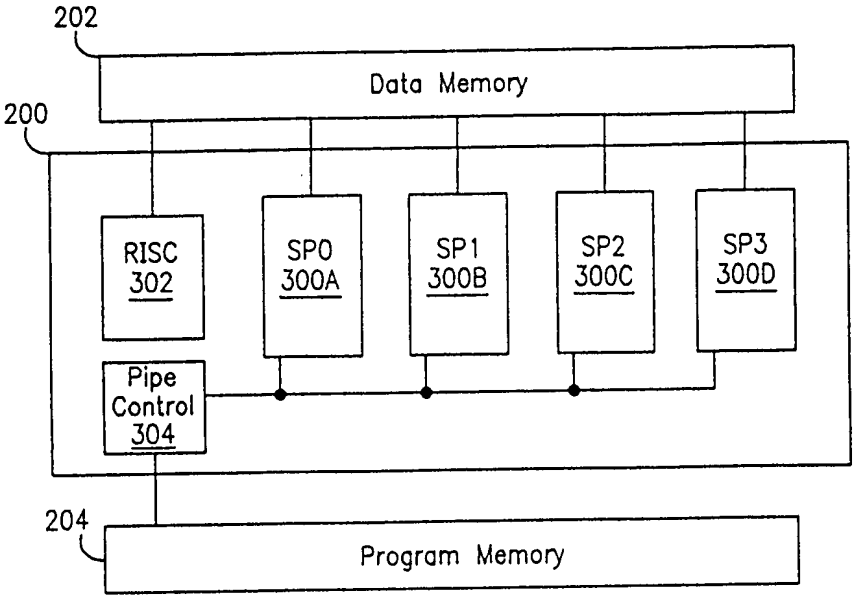

FIG. 3

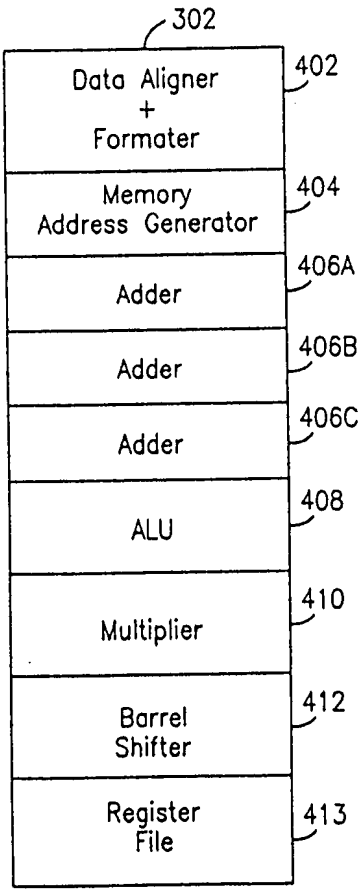

FIG. 4

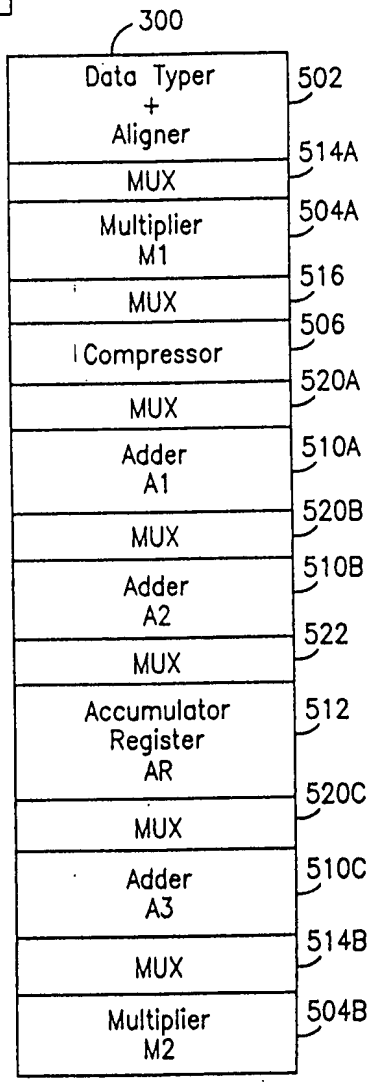

FIG. 5A

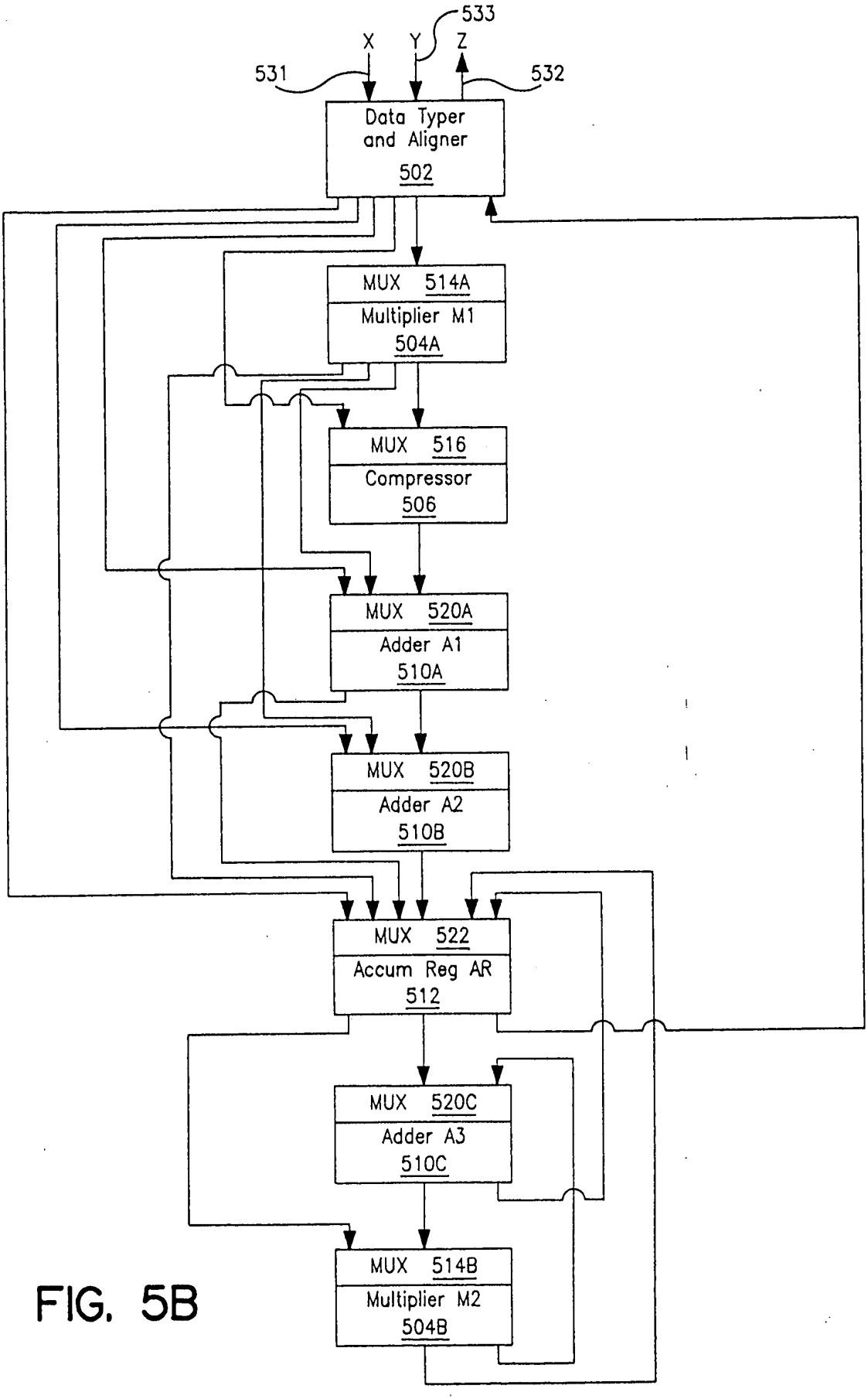
533
X
Y
Z
531
532
Data Typer and Aligner 502
MUX 514A
Multiplier M1 504A
MUX 516
Compressor 506
MUX 520A
Adder A1 510A
MUX 520B
Adder A2 510B
MUX 522
Accum Reg AR 512
MUX 520C
Adder A3 510C
MUX 514B
Multiplier M2 504B

FIG. 5B

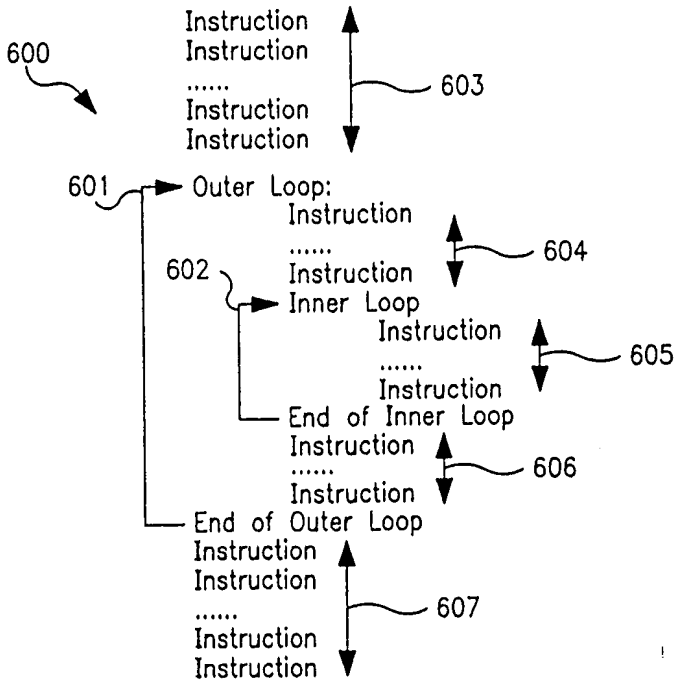
600
Instruction
Instruction
.....
Instruction
Instruction
603
601
Outer Loop:
Instruction
.....
Instruction
604
602
Inner Loop
Instruction
.....
Instruction
605
End of Inner Loop
Instruction
.....
Instruction
606
End of Outer Loop
Instruction
Instruction
.....
Instruction
Instruction
607

FIG. 6A

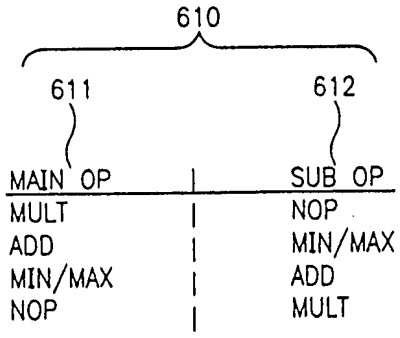
610
611
612
MAIN OP
SUB OP
MULT
NOP
ADD
MIN/MAX
MIN/MAX
ADD
NOP
MULT

FIG. 6B

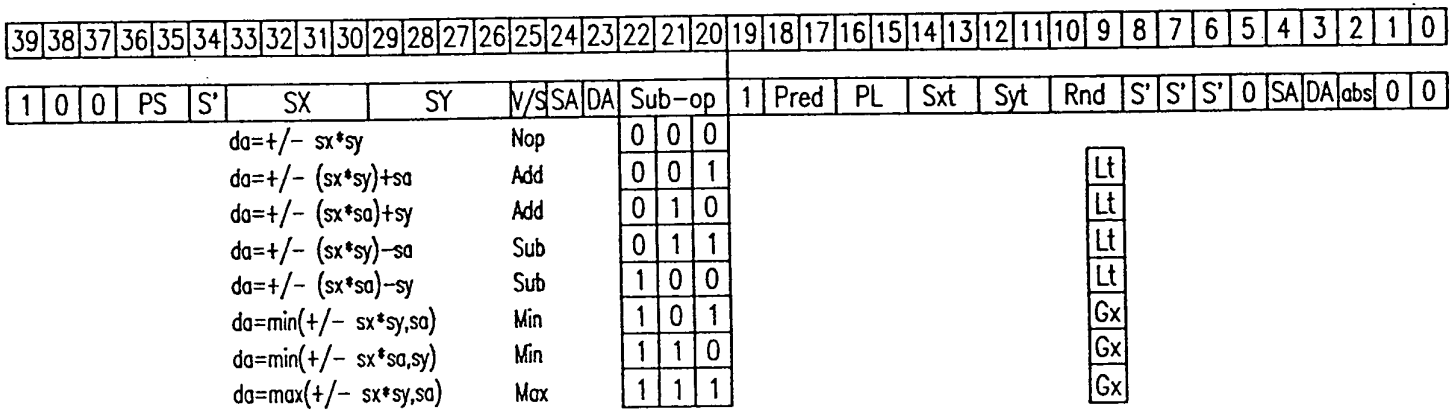

FIG. 6C

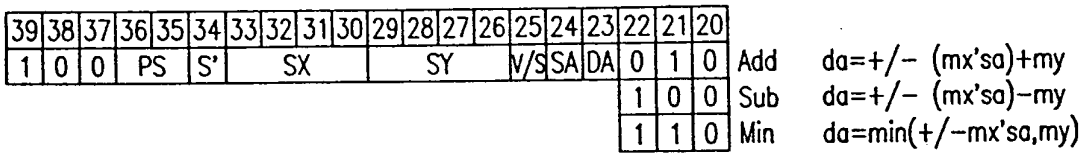

FIG. 6D

Blakely, Sokoloff, Taylor & Zafman LLP (714) 557-3800
Title: Instruction Set Architecture for Signal Processors
1st Named Inventor: Kumar Ganapathy
Application No.: 10/666,570 Docket No.: 42P14031D2D
Sheet: 7 of 16

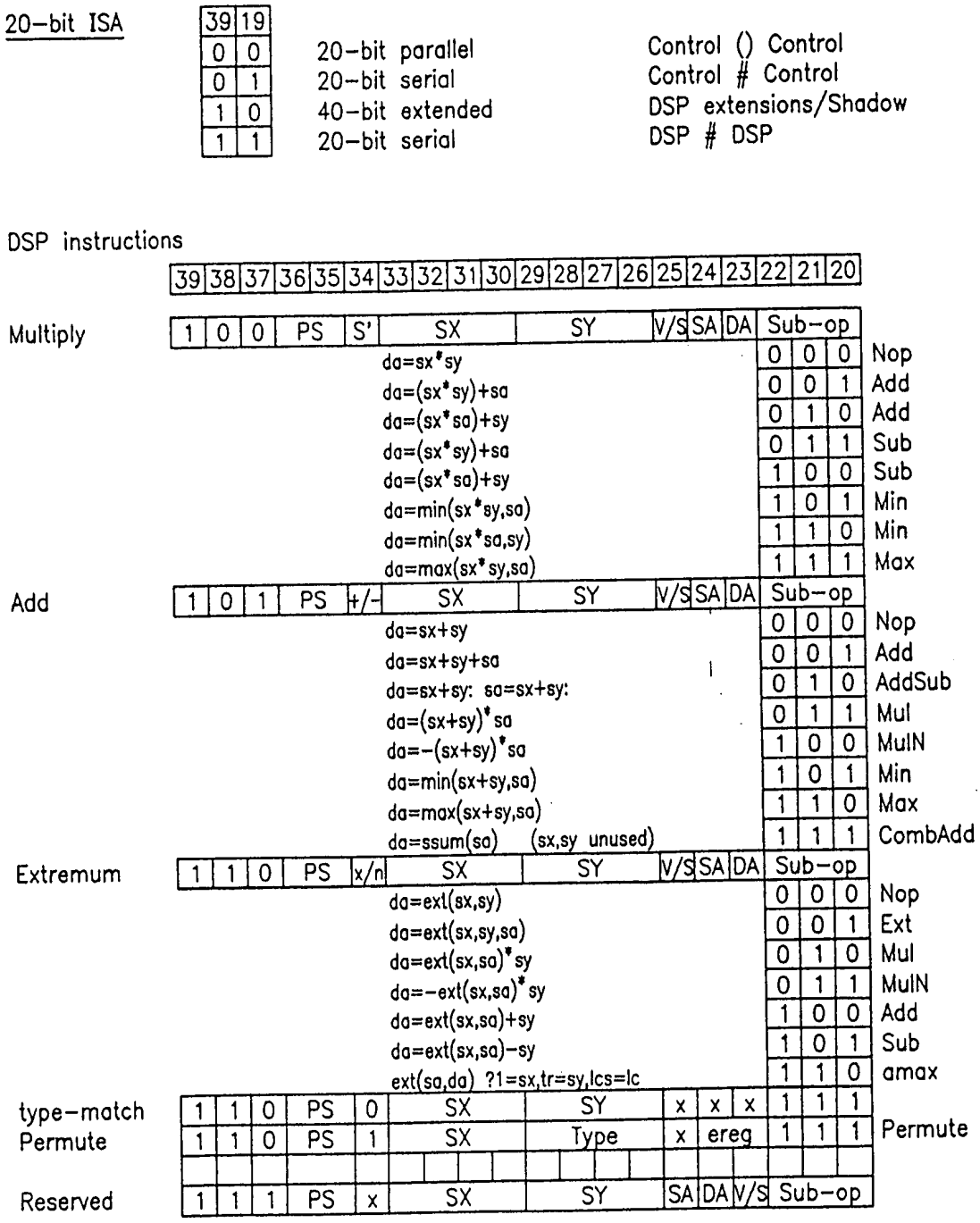
20-bit ISA
39 19
0 0 20-bit parallel
0 1 20-bit serial
1 0 40-bit extended
1 1 20-bit serial
Control () Control
Control # Control
DSP extensions/Shadow
DSP # DSP
DSP instructions
39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20
Multiply
1 0 0 PS S' SX SY V/S SA DA Sub-op
da=sx*sy 0 0 0 Nop
da=(sx*sy)+sa 0 0 1 Add
da=(sx*sa)+sy 0 1 0 Add
da=(sx*sy)+sa 0 1 1 Sub
da=(sx*sa)+sy 1 0 0 Sub
da=min(sx*sy,sa) 1 0 1 Min
da=min(sx*sa,sy) 1 1 0 Min
da=max(sx*sy,sa) 1 1 1 Max
Add
1 0 1 PS +/- SX SY V/S SA DA Sub-op
da=sx+sy 0 0 0 Nop
da=sx+sy+sa 0 0 1 Add
da=sx+sy: sa=sx+sy: 0 1 0 AddSub
da=(sx+sy)*sa 0 1 1 Mul
da=-(sx+sy)*sa 1 0 0 MulN
da=min(sx+sy,sa) 1 0 1 Min
da=max(sx+sy,sa) 1 1 0 Max
da=ssum(sa) (sx,sy unused) 1 1 1 CombAdd
Extremum
1 1 0 PS x/n SX SY V/S SA DA Sub-op
da=ext(sx,sy) 0 0 0 Nop
da=ext(sx,sy,sa) 0 0 1 Ext
da=ext(sx,sa)*sy 0 1 0 Mul
da=-ext(sx,sa)*sy 0 1 1 MulN
da=ext(sx,sa)+sy 1 0 0 Add
da=ext(sx,sa)-sy 1 0 1 Sub
ext(sa,da) ?1=sx,tr=sy,lcs=lc 1 1 0 amax
type-match
1 1 0 PS 0 SX SY x x x 1 1 1
Permute
1 1 0 PS 1 SX Type x ereg 1 1 1 Permute
Reserved
1 1 1 PS x SX SY SA DA V/S Sub-op

FIG. 6E-1

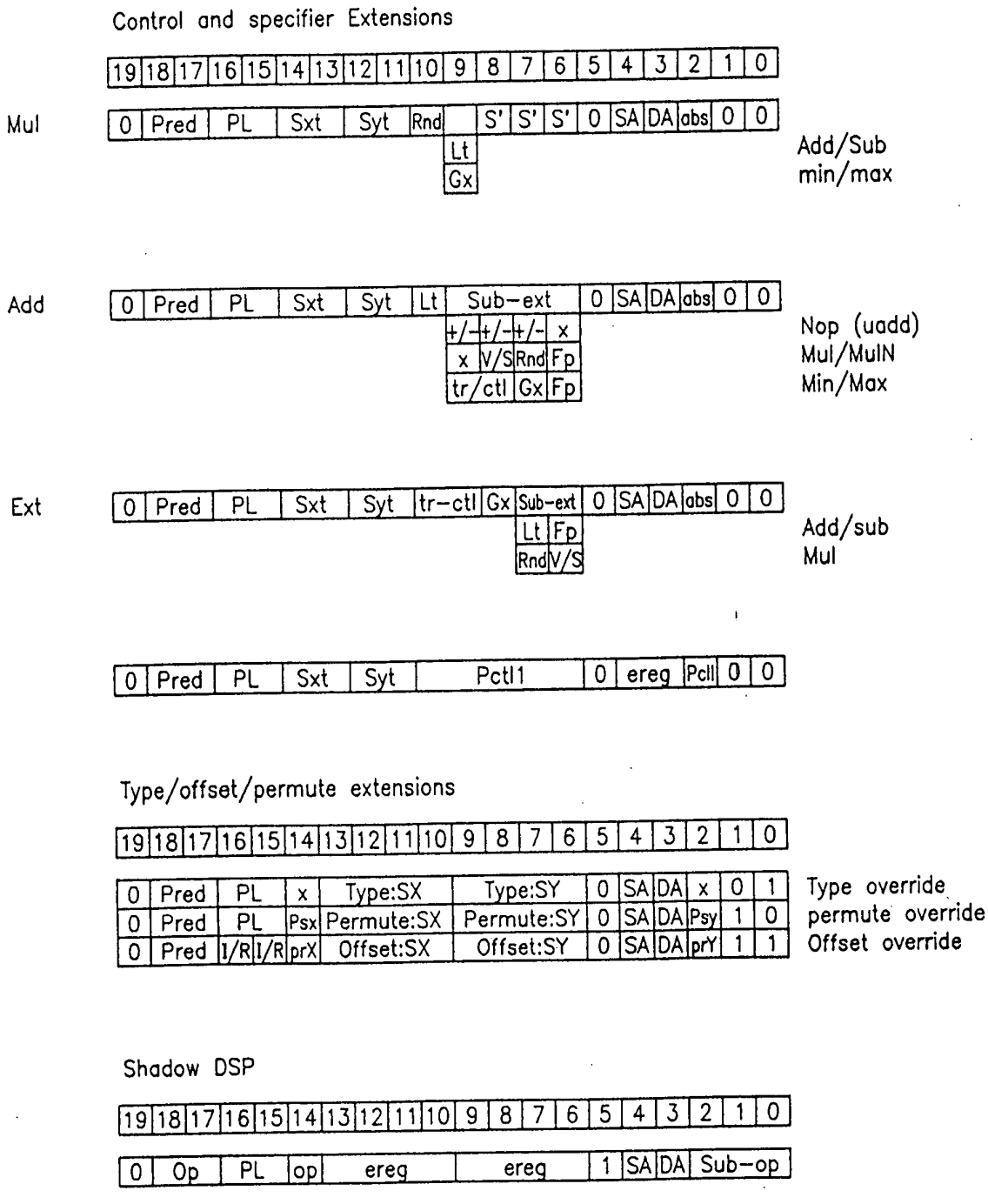
Control and specifier Extensions
19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Mul
0 Pred PL Sxt Syt Rnd S' S' S' 0 SA DA abs 0 0
Lt
Gx
Add/Sub
min/max
Add
0 Pred PL Sxt Syt Lt Sub-ext 0 SA DA abs 0 0
+/- +/- +/- x
x V/S Rnd Fp
tr/ctl Gx Fp
Nop (uadd)
Mul/MulN
Min/Max
Ext
0 Pred PL Sxt Syt tr-ctl Gx Sub-ext 0 SA DA abs 0 0
Lt Fp
Rnd V/S
Add/sub
Mul
0 Pred PL Sxt Syt Pctl1 0 ereg Pcll 0 0
Type/offset/permute extensions
19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 Pred PL x Type:SX Type:SY 0 SA DA x 0 1
0 Pred PL Psx Permute:SX Permute:SY 0 SA DA Psy 1 0
0 Pred I/R I/R prX Offset:SX Offset:SY 0 SA DA prY 1 1
Type override
permute override
Offset override
Shadow DSP
19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 Op PL op ereg ereg 1 SA DA Sub-op

FIG. 6E-2

Control instructions

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
add,sub	L	Pred		0	0	0	RX				RY				RZ				+/-	0	
max,min	L	Pred		0	0	0	RX				RY				RZ				X/N	1	
Shift	L	Pred		0	0	1	RX				UI4				RZ				UI2	R/L	<Bit1,Bits9-6>
Logic	L	Pred		0	1	0	RX				RY				RZ				&,	&1	==UI5 (Shift
Mux	L	Pred		0	1	1	RX				RY				RZ				Pd	0	Amount)
mov	L	Pred		0	1	1	RX				DZ				Rxt	Dzl	0	0	0	1	
addi	L	Pred		0	1	1	SI4				DZ				x	x	1	0	0	1	
mov2erg	L	Pred		0	1	1	RX				unit		ereg		qd	type		1	0	1	
l.dm	L	Pred		0	1	1	RX				DZ1				DZ2				1	1	
Set4bits	L	Pred		1	0	0	UI4:POS				RZ				Rzt	UI4				0	
Set2bits	L	Pred		1	0	0	UI4:POS				RZ				Rzt	UI2		0	0	1	
Setbit	L	Pred		1	0	0	UI4:POS				RZ				Rzt	UI1	UI1	1	0	1	<Bit3,Bits13-
Movi	L	Pred		1	0	0	SI8								RZ				1	1	10>==UI5 POS
Jmp	L	Pred		1	0	1	SI9								0	PRED			0	0	
Call	L	Pred		1	0	1	SI9								1	PRED			0	0	
Loop	L	Pred		1	0	1	UI5:Lcount				UI5:Lsize							UI2:Lst	0	1	
Jmpi	L	Pred		1	0	1	RX				x	x	x	x	x	0	PRED		1	0	
Calli	L	Pred		1	0	1	RX				x	x	x	x	x	1	PRED		1	0	
Loopi	L	Pred		1	0	1	RX				x	UI5:Lsize						UI2:Lst	1	1	
Test	L	Pred		1	1	0	RX				RY				PZ			=,<,>		0	
Testbit	L	Pred		1	1	0	RX				UI5				PZ			B	0	1	
Andp, orp	L	Pred		1	1	0	Pa				Pb			Pc	PZ			&	1	1	
Load	L	Pred		1	1	1	MX				RZ				Ext				0	0	0
Store	L	Pred		1	1	1	MZ				RZ				Ext				1	0	0
eLoad	L	Pred		1	1	1	MX				RY				1	1	1	0	0	0	
eStore	L	Pred		1	1	1	MZ				RY				1	1	1	1	0	0	
Extended	L	Pred		1	1	1	Bits 27:16												1	0	
Logic2	L	Pred		1	1	1	RX				RY/RZ				Rxt	Ryt	&,1,&1,!		0	1	
mov-erg	L	Pred		1	1	1	unit		ereg		RZ				qd	Sft		0	1	1	
Crb	L	Pred		1	1	1	RX				RZ				s/m	0	0	1	1	1	
Panty	L	Pred		1	1	1	RX				PZ			0/E	0	1	0	1	1	1	
Stm	L	Pred		1	1	1	MZ				RX				1	1	0	1	1	1	
Abs	L	Pred		1	1	1	RX				RZ				0	0	1	1	1	1	
Neg	L	Pred		1	1	1	RX				RZ				0	1	1	1	1	1	
Div-step	L	Pred		1	1	1	RX				RZ				1	0	1	1	1	1	
Test&Set	L	Pred		1	1	1	RX				PZ			0	1	1	1	1	1	1	
Reserved	L	Pred		1	1	1					0	0	1		1	1	1	1	1	1	
Return	L	Pred		1	1	1	Pred		I-ctl		0	1	0	1	1	1	1	1	1	1	
Zero-ac	L	Pred		1	1	1	ac #				1	1	0	1	1	1	1	1	1	1	
eSync	L	Pred		1	1	1	RZ				0	1	1	1	1	1	1	1	1	1	
Swi	L	Pred		1	1	1	UI3			0	1	1	1	1	1	1	1	1	1	1	
Nop	L	Pred		1	1	1	UI3			1	1	1	1	1	1	1	1	1	1	1	

FIG. 6F

Extended Control

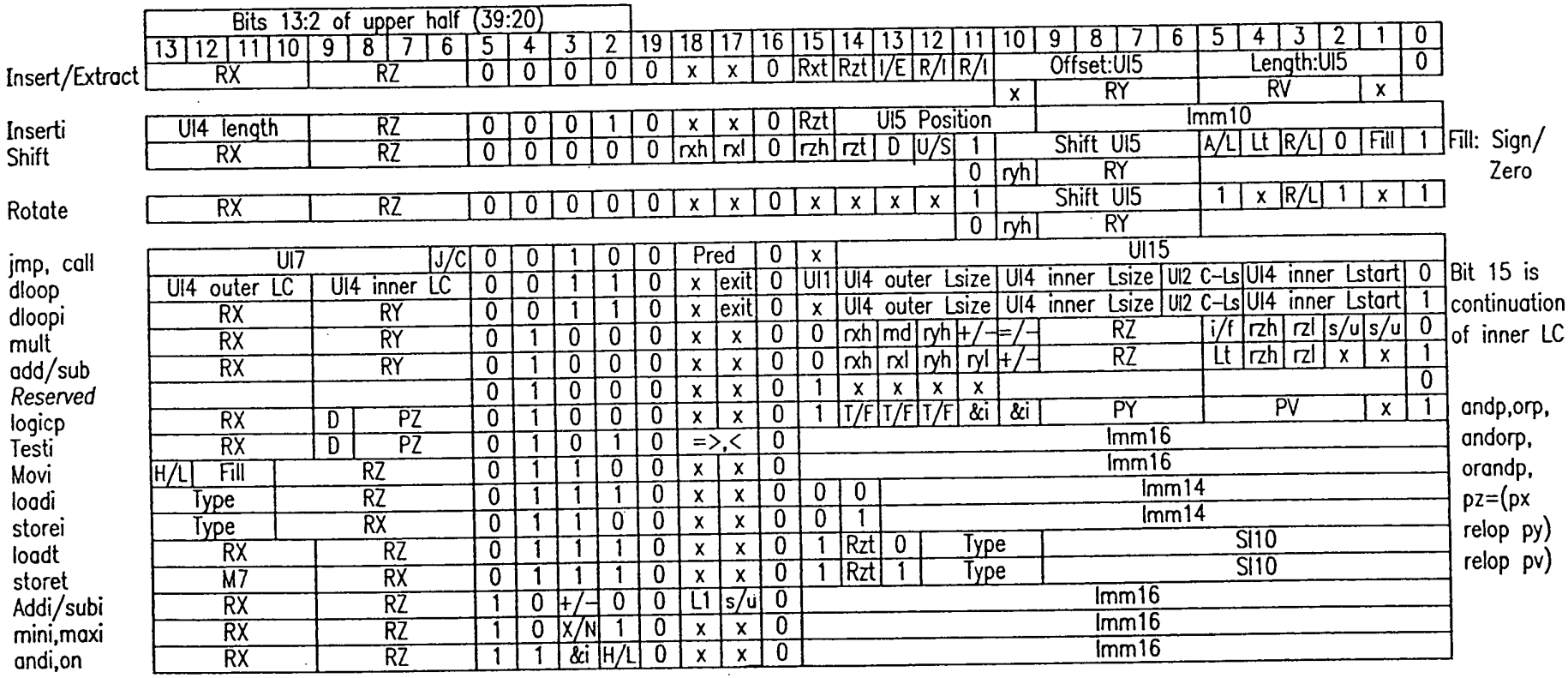

FIG. 6G

Blakely, Sokoloff, Taylor & Zafman LLP (714) 557-3800
Title: Instruction Set Architecture for Signal Processors
1st Named Inventor: Kumar Ganapathy
Application No.: 10/666,570 Docket No.: 42P14031D2D
Sheet: 11 of 16

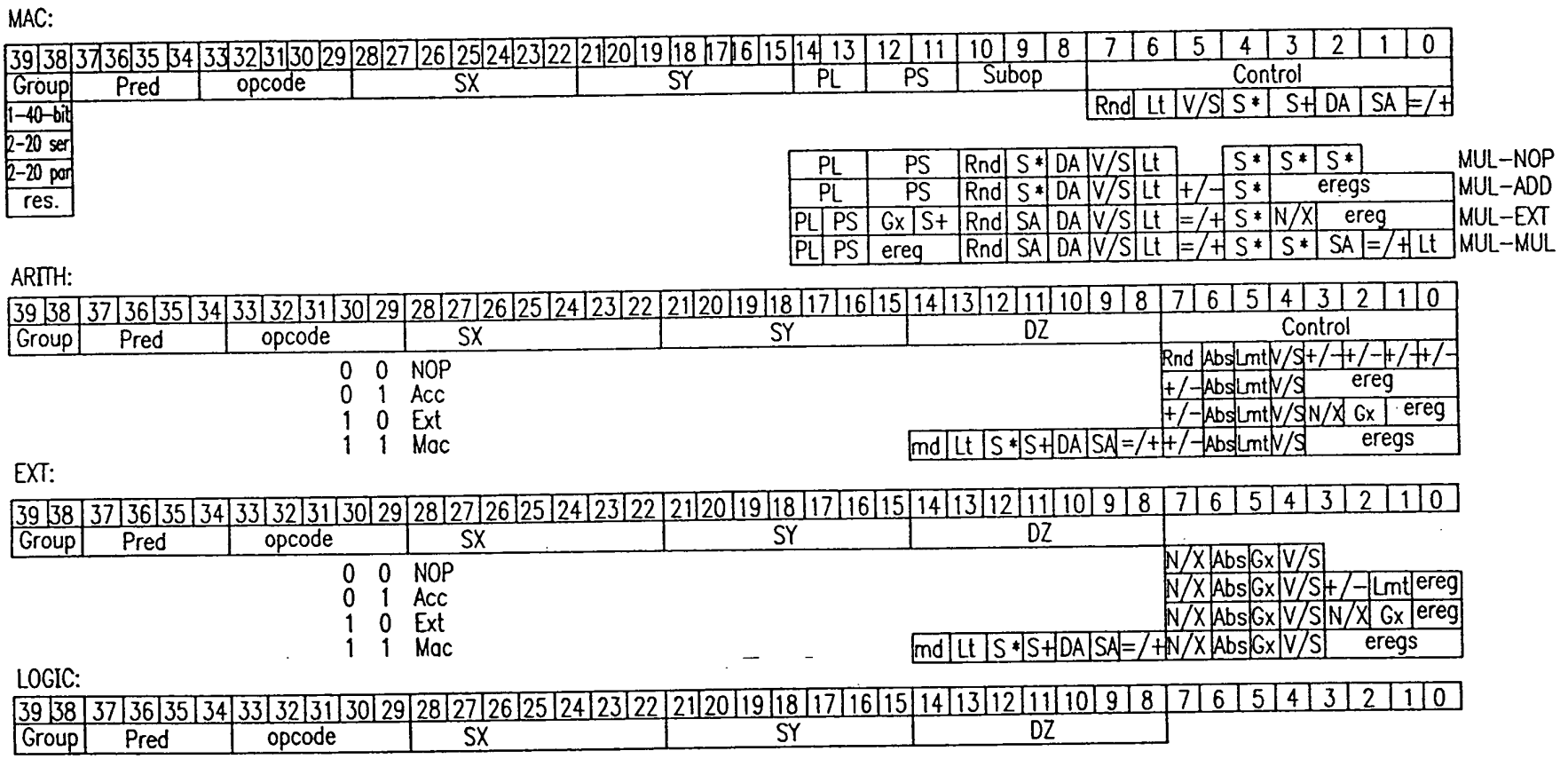
MAC:
39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Group
Pred
opcode
SX
SY
PL
PS
Subop
Control
Rnd Lt V/S S* S+ DA SA =/+
1-40-bit
2-20 ser
2-20 par
res.
PL PS Rnd S* DA V/S Lt S* S* S* MUL-NOP
PL PS Rnd S* DA V/S Lt +/− S* eregs MUL-ADD
PL PS Gx S+ Rnd SA DA V/S Lt =/+ S* N/X ereg MUL-EXT
PL PS ereg Rnd SA DA V/S Lt =/+ S* S* SA =/+ Lt MUL-MUL
ARITH:
Group
Pred
opcode
SX
SY
DZ
Control
Rnd Abs Lmt V/S +/− +/− +/− +/−
+/− Abs Lmt V/S ereg
+/− Abs Lmt V/S N/X Gx ereg
md Lt S* S+ DA SA =/+ +/− Abs Lmt V/S eregs
0 0 NOP
0 1 Acc
1 0 Ext
1 1 Mac
EXT:
N/X Abs Gx V/S
N/X Abs Gx V/S +/− Lmt ereg
N/X Abs Gx V/S N/X Gx ereg
md Lt S* S+ DA SA =/+ N/X Abs Gx V/S eregs
LOGIC:

FIG. 6H-I

Shift:

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Group		Pred				opcode				SX								DZ							Amount						PL		PS	Lt	Rot	Fill	A/L	1	1	Shift
Group		Pred				opcode				SX								DZ							Amount					Position						I/E	0	1	Insert/extract
Group		Pred		Imm2		opcode				DZ						Imm14												Length				Position						0	Setbits

Immediate:

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group		op		DZ				Imm32																															
Group		opcode				SX						DZ						Subop		Imm16																			

Subop
MOV
ADD
SUB
MIN
MAX
AND
OR

Test:

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group		Pred				opcode					SX							SY							DPz			Subop												

Branch:

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group		Pred				opcode														Imm20																				

Misc:

FIG. 6H-2

7-bit specifier Parallel Store, Parallel Load in DSP instructions

6	5	4	3	2	1	0

M/R

0	0	0	SPR s0–s15	
0	0	1	reserved	
0	1	0	ac–names	
0	1	1	gpr: r0–r15	
1	0	ptr: (ro) to (r15)		off
1	1	offset: UI4		off

Mem[ptr]||ptr +=idx Always postupdate
Mem[ptr + idx] ptr:p14,p15 Always postupdate

6-bit specifier DSP instructions

5	4	3	2	1	0

M/R

0	0	ac–names	
0	1	gpr: r0–r15	
1	ptr: (r0) to (r15)		off

Always postupdate

5-bit specifier RISC instructions

4	3	2	1	0

0	spr: s0–s15
1	gpr: r0–r15

4-bit specifier

3	2	1	0

gpr: r0–r15	
ptr: (r0–r7)	off
ereg	

RISC instructions
20–bit DSP instructions
20–bit Shadow DSP instructions

AP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
type				permute					CB	idx1: UI3 (0–7)			xhr0: Si5 (–16to15)					pl															

FIG. 6I-I

ac-names

3	2	1	0			SPR:
0	0	0	0	A0	(use type, SIMD)	gpr-type
0	0	0	1	A1		ereg type
0	0	1	0	T		fu-ctl
0	0	1	1	TR		pls-ctf
0	1	0	0	A00	(unit 0)	cb-ctl
0	1	0	1	A10		loop-ctl
0	1	1	0	T0		pcr
0	1	1	1	TR0		status
1	0	0	0	SX1		
1	0	0	1	SX1s		
1	0	1	0	SX2		
1	0	1	1	SX2s		
1	1	0	0	SY1		
1	1	0	1	SY1s		
1	1	1	0	SY2		
1	1	1	1	SY2s		

ereg names

3	2	1	0	
0	0	0	0	A0
0	0	0	1	A1
0	0	1	0	T
0	0	1	1	TR
0	1	0	0	PP0
0	1	0	1	Aout
0	1	1	0	PP1
0	1	1	1	Dout
1	0	0	0	SX1
1	0	0	1	SX1s
1	0	1	0	SX2
1	0	1	1	SX2s
1	1	0	0	SY1
1	1	0	1	SY1s
1	1	1	0	SY2
1	1	1	1	SY2s

FIG. 6I-2

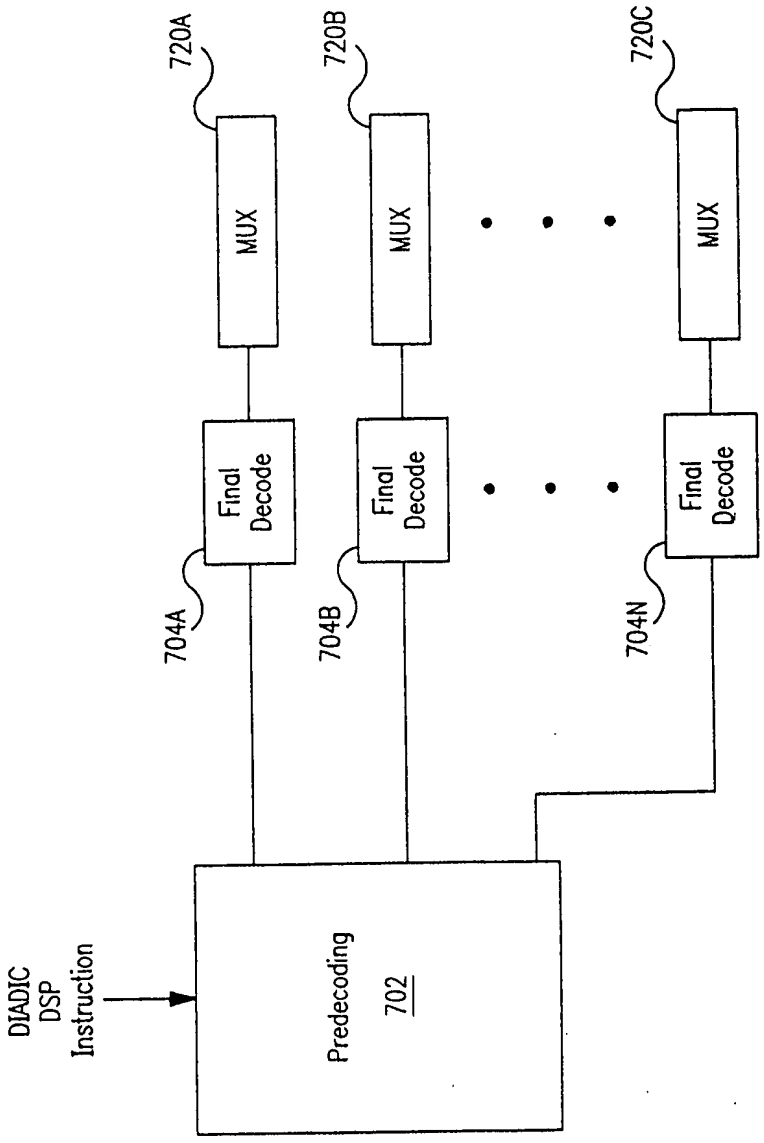
720A
720B
720C
MUX
MUX
MUX
Final Decode
Final Decode
Final Decode
704A
704B
704N
DIADIC DSP Instruction
Predecoding
702

FIG. 7